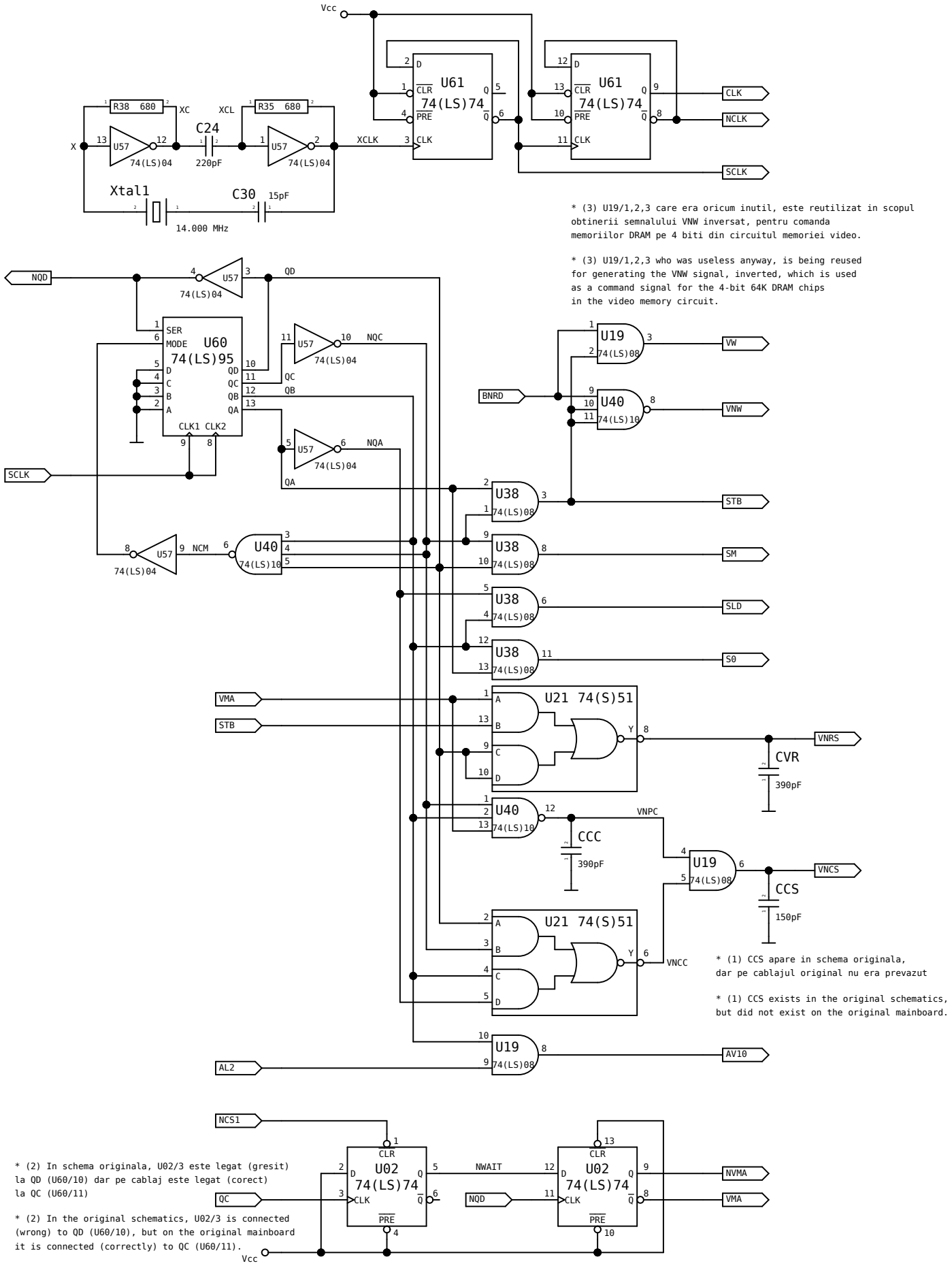
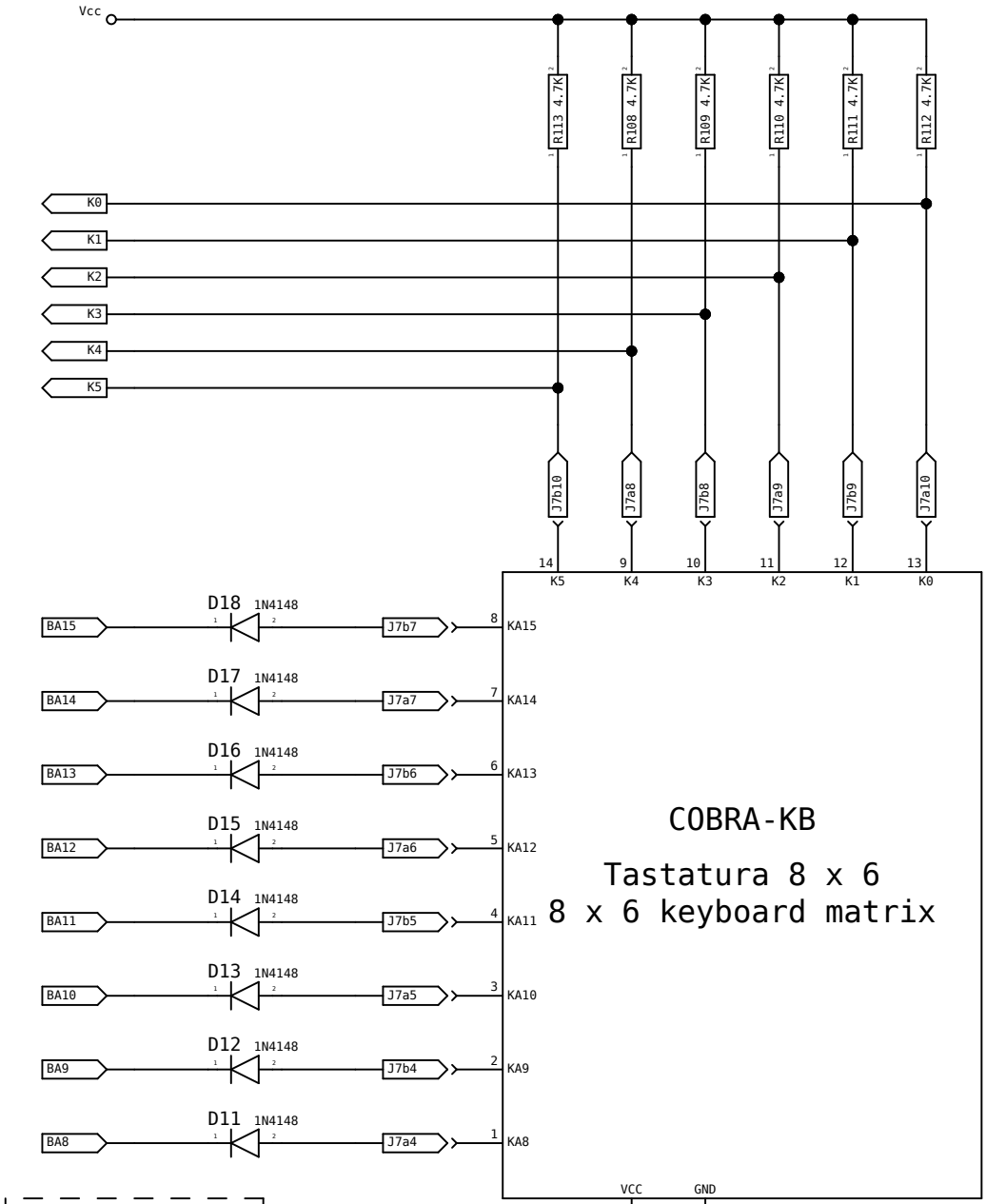
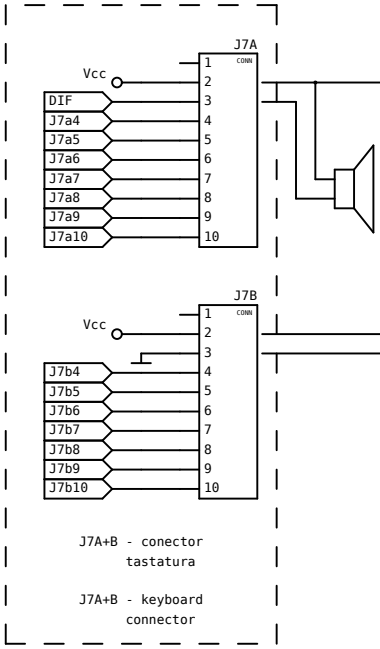


TITLE μC CoBra - Arbitrul de memorie si logica de comanda CoBra μC - Memory access prioritizer and command logic	
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 1 OF 18	DRAWN BY: ElectroNNix





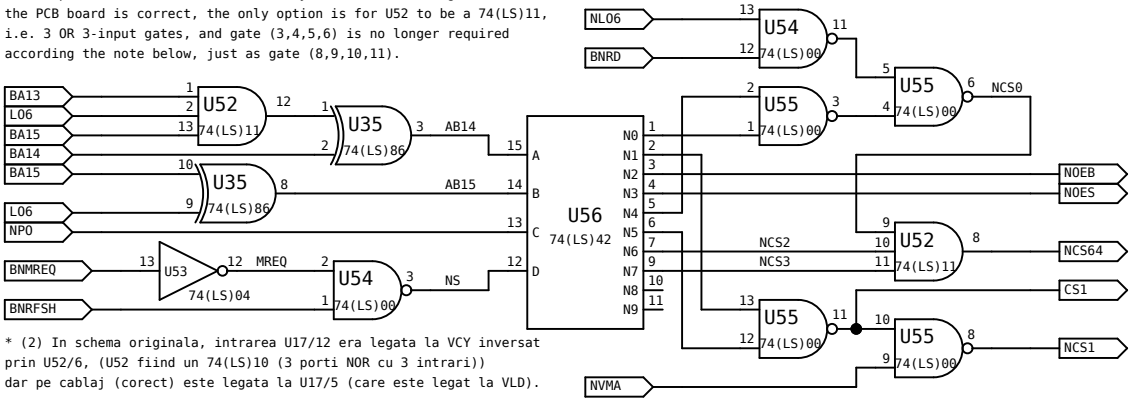
TITLE	µC CoBra - Circuitul de conectare tastatura CoBra µC - Keyboard interfacing circuit		
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	2 OF 18	DRAWN BY:	ElectroNNix

* (1) In schema originala, U52 era un 74(LS)10 (3 porti NOR cu 3 intrari), BA13, BA15 si L06 erau trecute prin U52/12,1,2,13 si apoi iesirea U52/12 era inversata prin poarta U52/8,9,10,11 folosita ca inversor, care mai departe era legata la U35/1. Pe cablaj, U52 are portile (3,4,5,6) si (8,9,10,11) nefolosite (pinii lasati in gol) iar iesirea U52/12 este legata direct la intrarea U35/1. Considerind cablajul corect, singura optiune este ca U52 sa fie un 74(LS)11, adica 3 porti OR cu cite 3 intrari, iar poarta (3,4,5,6) nu mai e necesara conform notei de mai jos, ca si poarta (8,9,10,11).

* (1) In the original schematics, U52 was a 74(LS)10 (3 NOR 3-input gates), BA13, BA15 and L06 were passed through U52/12,1,2,13 and then the output U52/12 was inverted through gate U52/8,9,10,11 used as inverter, which was further connected to U35/1. On the PCB board, U52 has the gates (3,4,5,6) and (8,9,10,11) unused (N.C. pins) and output U52/12 is connected directly to U35/1. Assuming the PCB board is correct, the only option is for U52 to be a 74(LS)11, i.e. 3 OR 3-input gates, and gate (3,4,5,6) is no longer required according the note below, just as gate (8,9,10,11).

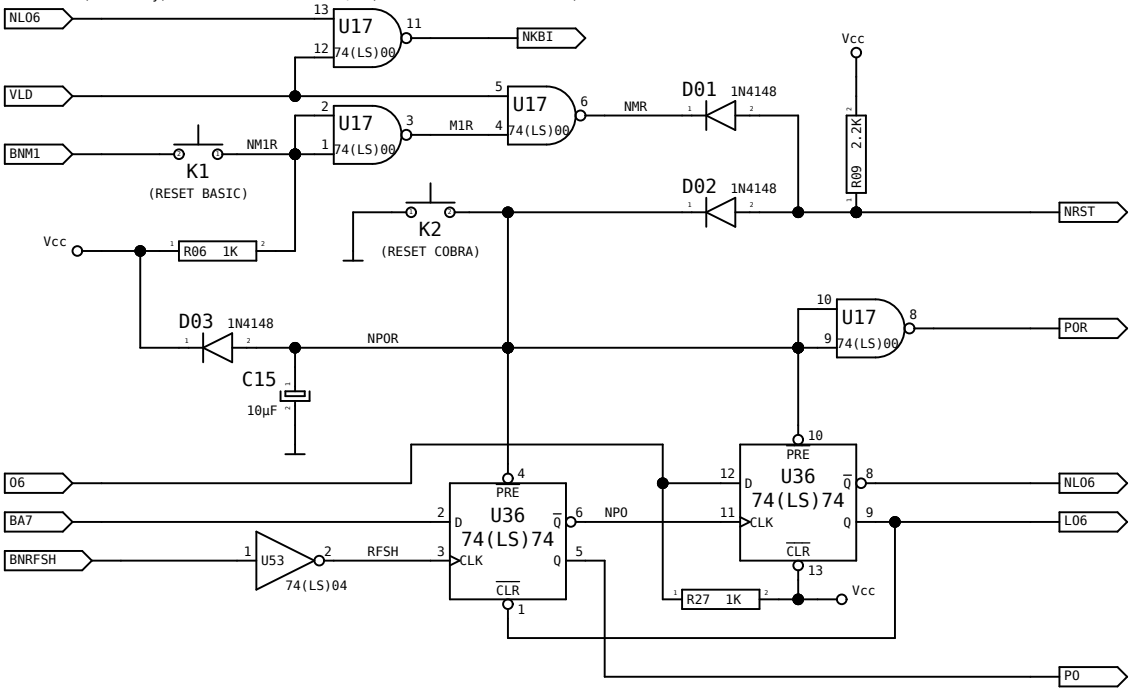
* (3) Poarta U52/8,9,10,11 care era neconectata, este acum folosita pentru "modificarea de 64K" (1 banc memorii DRAM 64K in loc de 3 bancuri (#0, #2, #3) de memorii DRAM 16K). Restul modificarii este realizat in "Circuitul memoriei dinamice - pag.1/2".

* (3) Gate U52/8,9,10,11 which was disconnected, is now used for the "64K modification" (1 bank of DRAM 64K chips instead of 3 banks (#0, #2, #3) of DRAM 16K chips). The rest of the modification is at the "Dynamic memory circuit - pag.1/2".



* (2) In schema originala, intrarea U17/12 era legata la VCY inversat prin U52/6, (U52 fiind un 74(LS)10 (3 porti NOR cu 3 intrari)) dar pe cablaj (corect) este legata la U17/5 (care este legat la VLD).

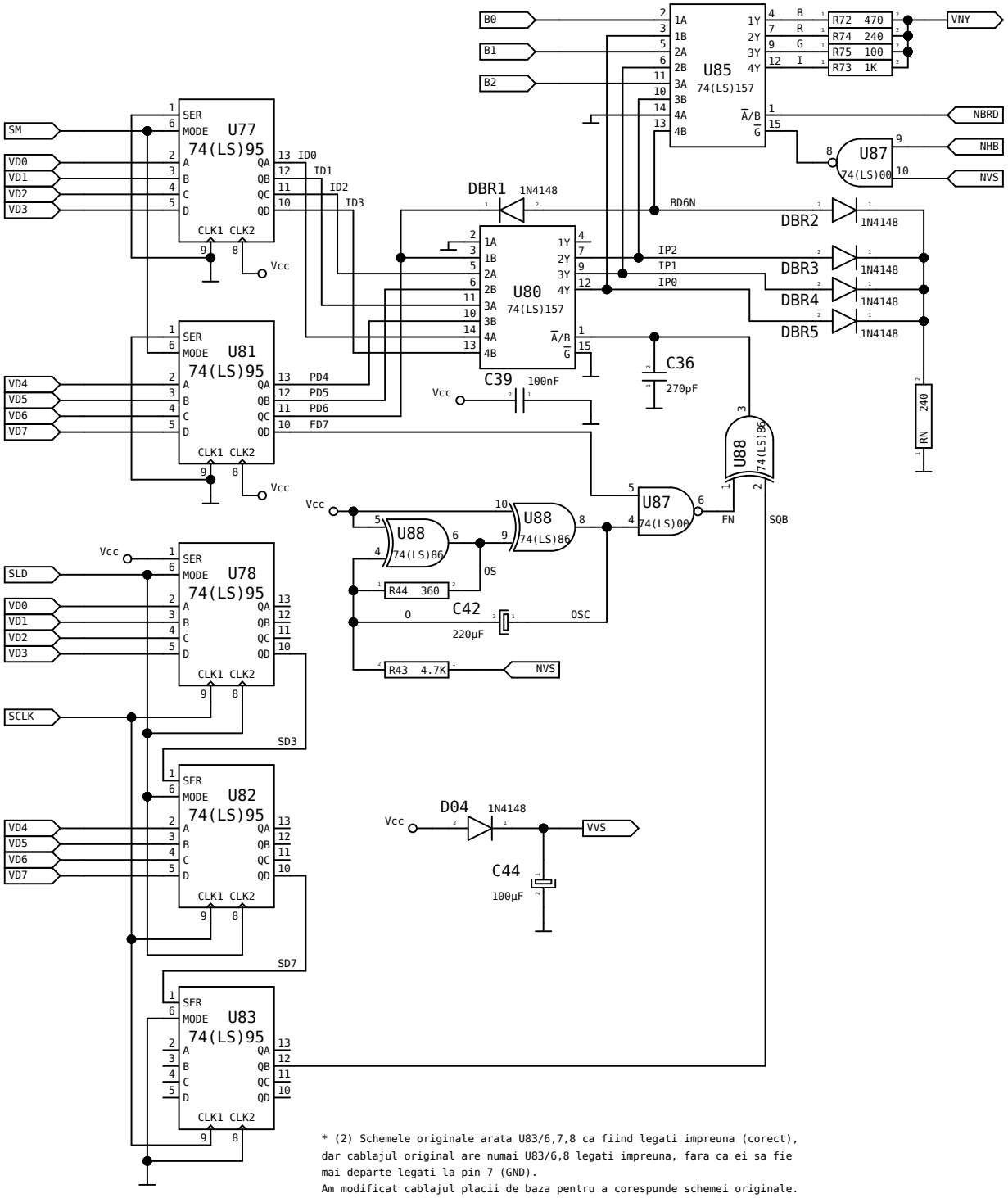
* (2) In the original schematics, input U17/12 was connected to VCY inverted through U52/6, (U52 being a 74(LS)10 (3 NOR 3-input gates)) but on the PCB board (correctly) it is connected to U17/5 (which is connected to VLD).



TITLE µC CoBra - Circuitul de configurare si selectie CoBra µC - Configurator and selector circuit	
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 3 OF 18	DRAWN BY: ElectroNNix

* (1) In schema originala, diodele DBR1-5 si rezistenta RN sint desenate
(cu toate ca diodele nu sint denumite) dar pe cablajul original nu sint prevazute,
iar U85/13 este legat direct la U80/3. Ca urmare, cablajul original nu permitea
functia de BRIGHT. Am modificat cablajul adaugind gauri pentru BDR1-5 si RN
si intrerupind deci legatura directa dintre U85/13 si U80/3.

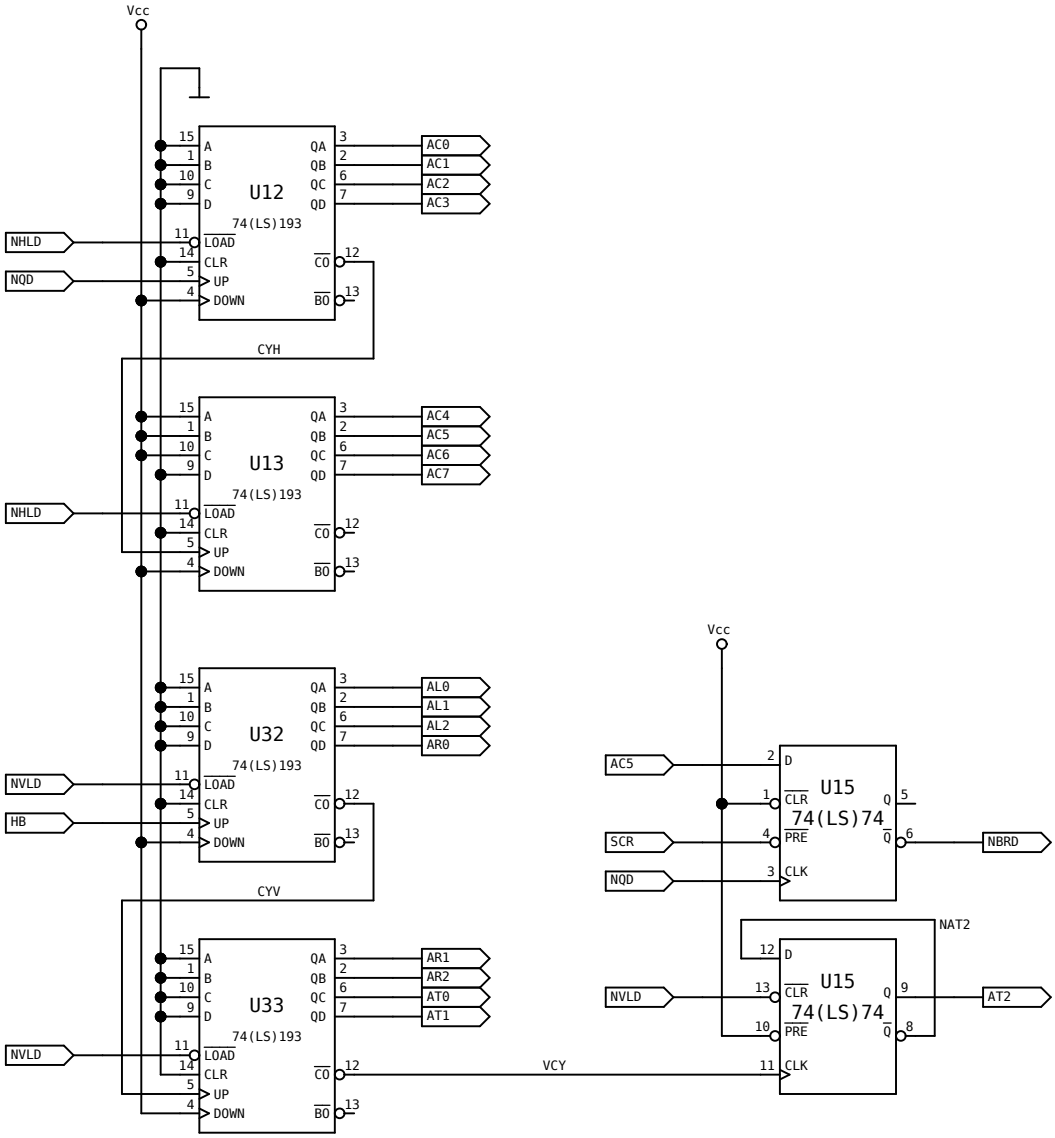
* (1) In the original schematics, diodes DBR1-5 and resistor RN are drawn
(although the diodes don't have names) but on the original mainboard they are not placed,
and U85/13 is directly connected to U80/3. Therefore, the original mainboard would not
allow the BRIGHT function. I have modified the mainboard layout by adding mounting holes for
BDR1-5 and RN and therefore interrupting the direct connection between U85/13 and U80/3.



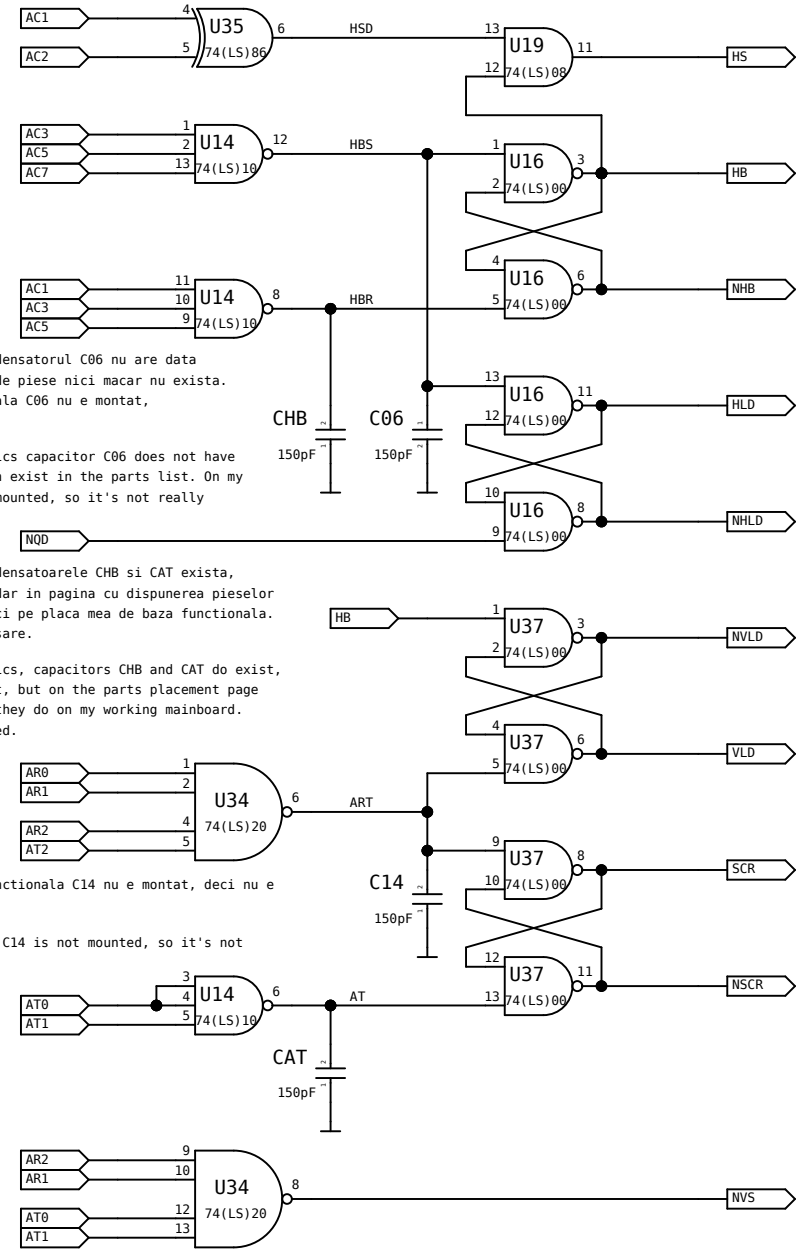
* (2) Schemele originale arata U83/6,7,8 ca fiind legati impreuna (corect),
dar cablajul original are numai U83/6,8 legati impreuna, fara ca ei sa fie
mai departe legati la pin 7 (GND).
Am modificat cablajul placii de baza pentru a corespunde schemei originale.
(Vezi legatura #25 fata 2)

* (2) The original schematics show U83/6,7,8 connected together (correctly),
but the original mainboard layout only has U83/6,8 connected together
without them being further connected to pin 7 (GND).
I have modified the mainboard layout to match the original schematics.
(See rewiring #25 side 2)

TITLE	µC CoBra - Circuitul formator semnal video CoBra µC - Video signal generator circuit
FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 4 OF 18	DRAWN BY: ElectroNNix



TITLE	µC CoBra - Circuitul de generare adrese video CoBra µC - Video address generator circuit		
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	5 OF 18	DRAWN BY:	ElectroNNix



* (1) In schema originala condensatorul C06 nu are data nici o valoare, iar in lista de piese nici macar nu exista. Pe placa mea de baza functionala C06 nu e montat, deci nu e intr-adevar necesar.

* (1) In the original schematics capacitor C06 does not have any value, and it doesn't even exist in the parts list. On my working mainboard C06 is not mounted, so it's not really required.

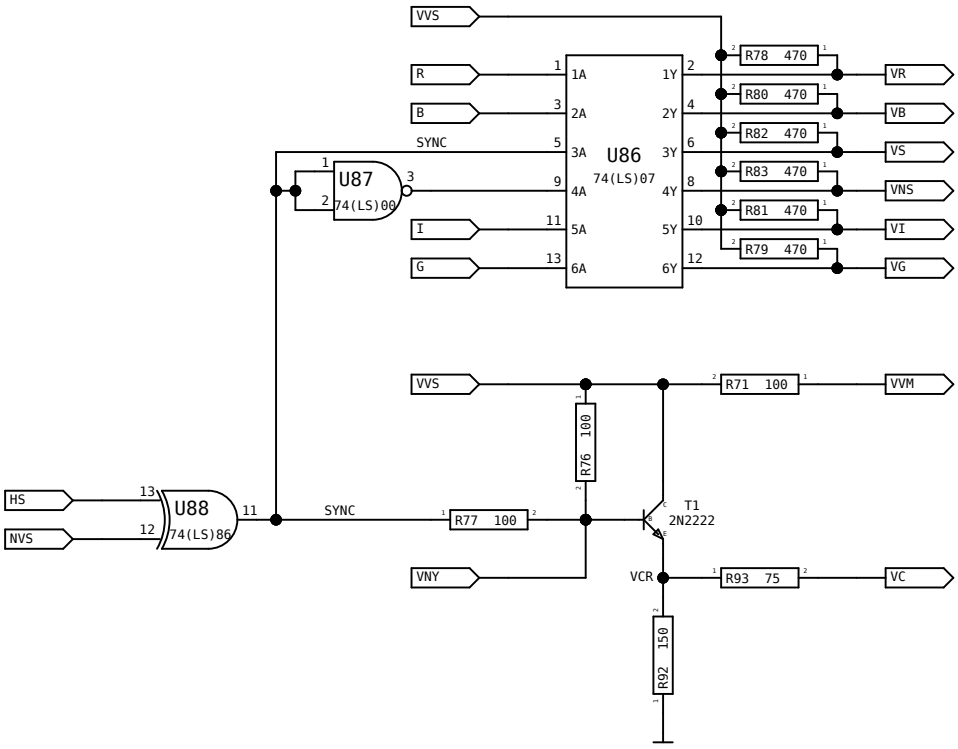
* (2) In schema originala condensatoarele CHB si CAT exista, exista si in lista de piese, dar in pagina cu dispunerea pieselor ele nu exista si nu exista nici pe placa mea de baza functionala. Deci nu sint intr-adevar necesare.

* (2) In the original schematics, capacitors CHB and CAT do exist, they also do in the parts list, but on the parts placement page they don't exist and neither they do on my working mainboard. So they are not really required.

* (3) Pe placa mea de baza functionala C14 nu e montat, deci nu e intr-adevar necesar.

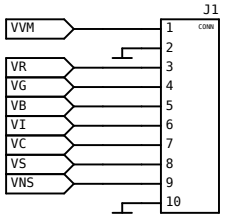
* (3) On my working mainboard C14 is not mounted, so it's not really required.

TITLE	µC CoBra - Circuitul generator de sincroimpulsuri CoBra µC - Video sync pulses generator circuit		
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	6 OF 18	DRAWN BY:	ElectroNNix



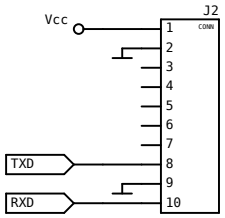
J1 - CONECTOR VIDEO

J1 - VIDEO CONNECTOR



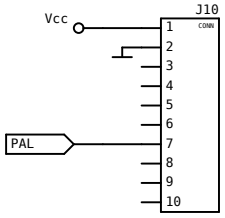
J2 - CONECTOR RS232

J2 - RS232 CONNECTOR



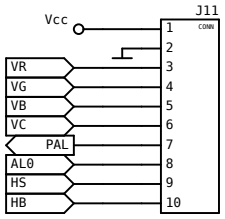
J10 - CONECTOR PAL VIDEO

J10 - PAL VIDEO CONNECTOR



J11 - CONECTOR CODOR PAL

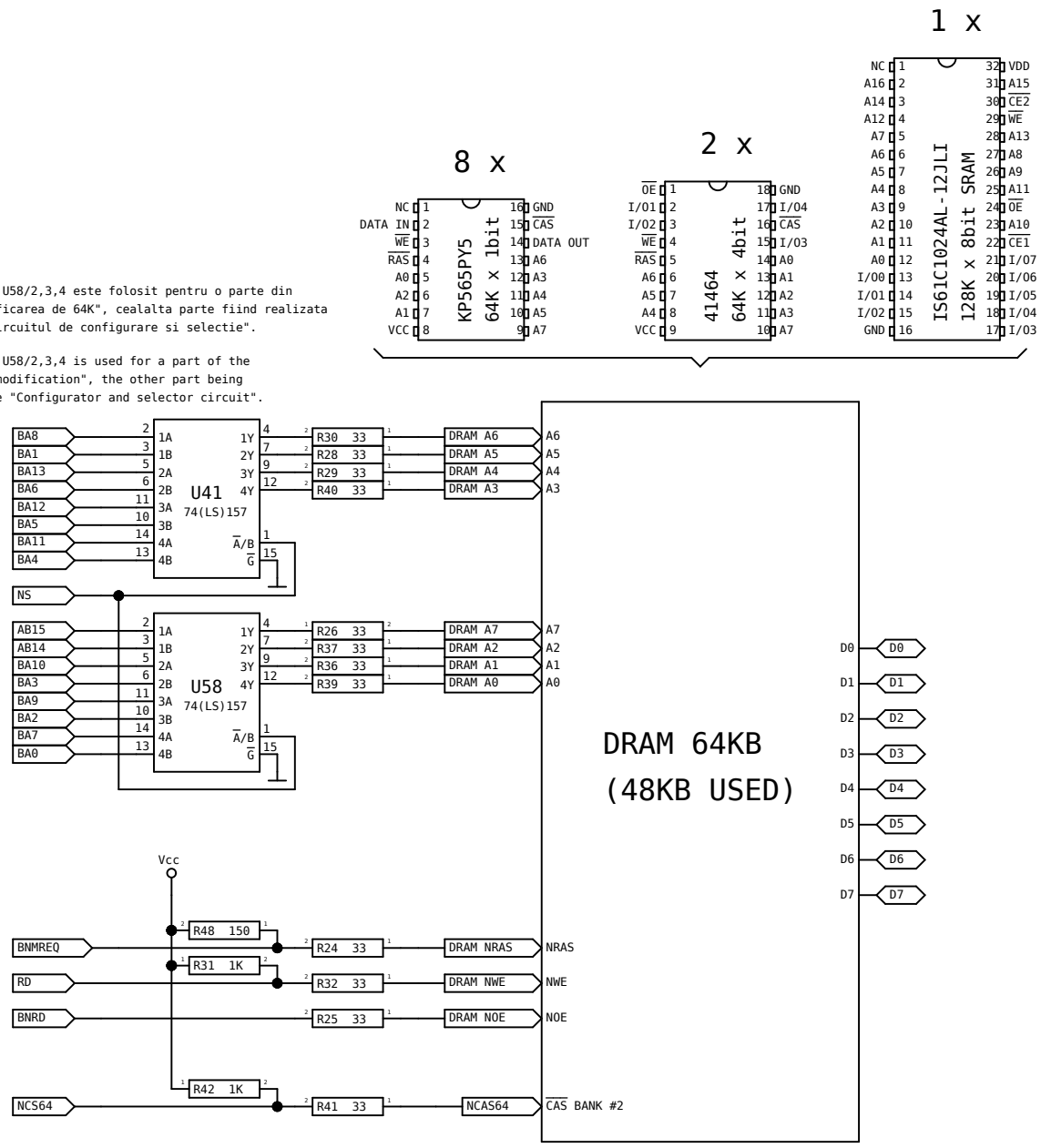
J11 - PAL CODER CONNECTOR



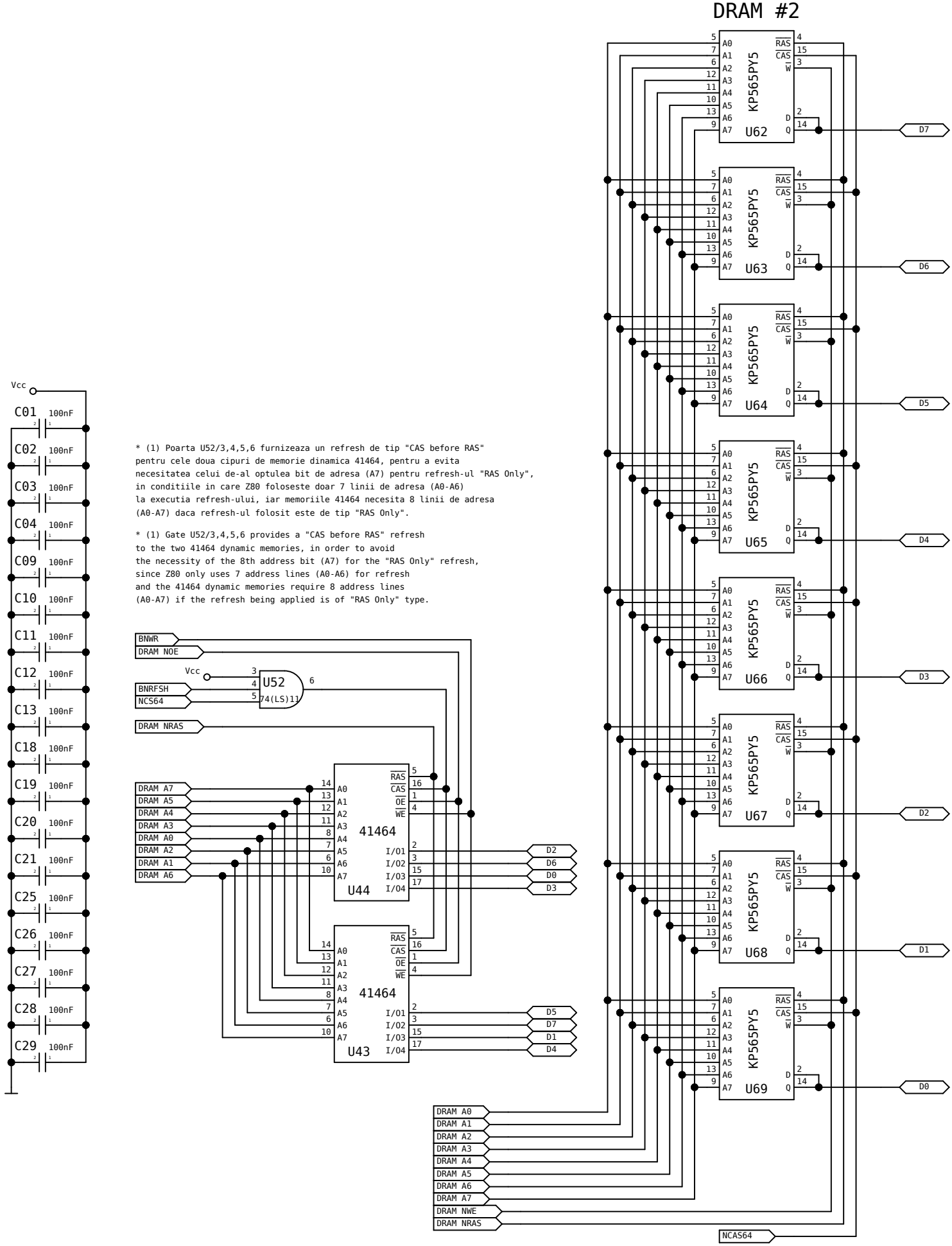
TITLE µC CoBra - Circuitul de interfata cu monitorul TV CoBra µC - TV monitor interfacing circuit	
FILE: CoBra	REVISION: 4.21 ROM upgrade, 64KB DRAM)
PAGE 7 OF 18	DRAWN BY: ElectroNNix

* (1) U58/2,3,4 este folosit pentru o parte din "modificarea de 64K", cealalta parte fiind realizata la "Circuitul de configurare si selectie".

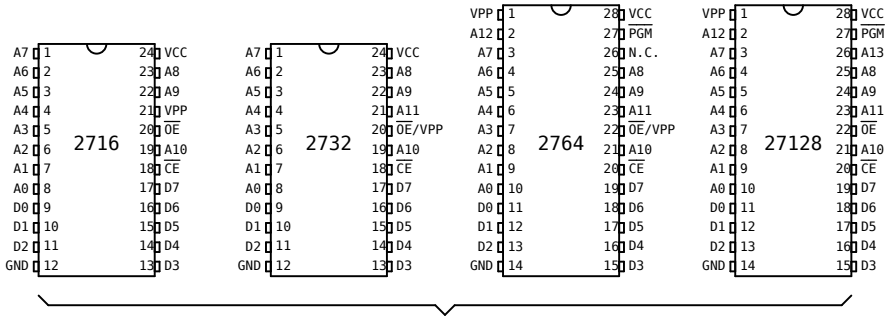
* (1) U58/2,3,4 is used for a part of the "64K modification", the other part being at the "Configurator and selector circuit".

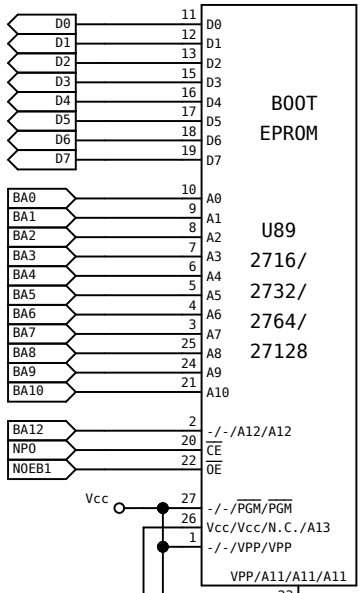


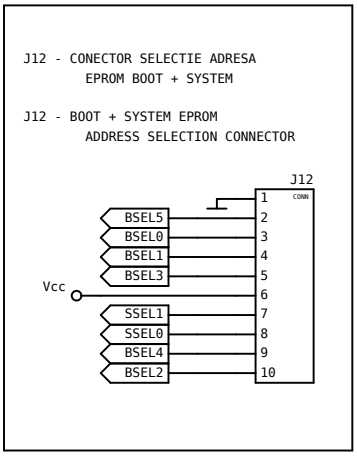
TITLE µC CoBra - Circuitul memoriei dinamice - pag.1/2 CoBra µC - Dynamic memory circuit - pag.1/2	
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 8 OF 18	DRAWN BY: ElectroNNix

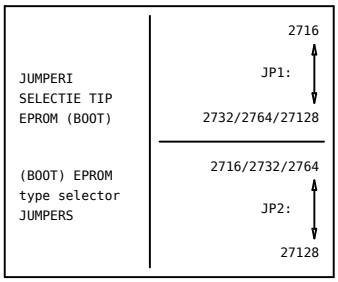


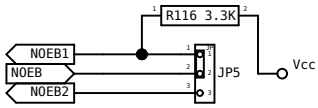
TITLE	µC CoBra - Circuitul memoriei dinamice - pag.2/2 CoBra µC - Dynamic memory circuit - pag.2/2	
FILE: CoBra		REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 9 OF 18		DRAWN BY: ElectroNNix

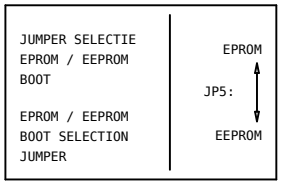


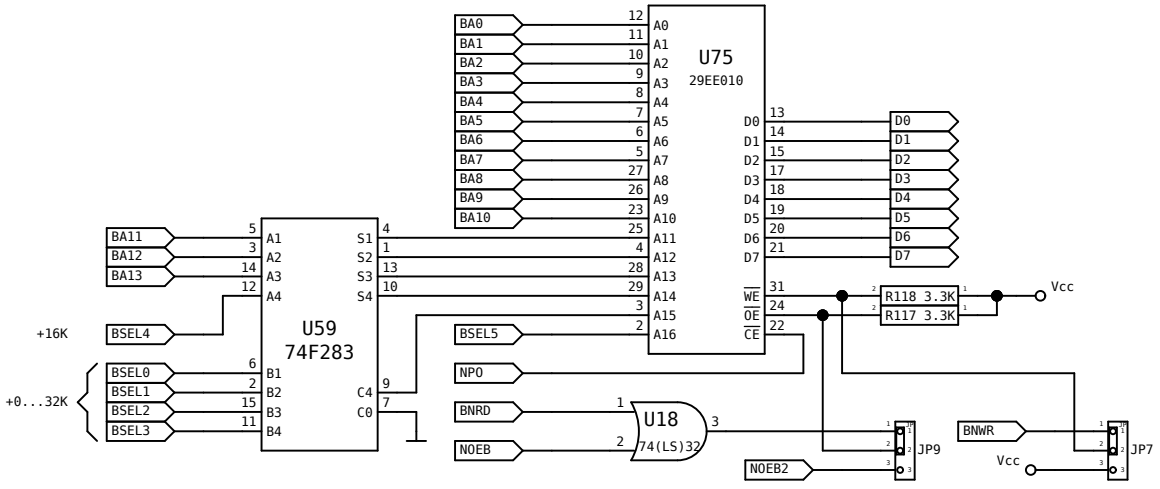


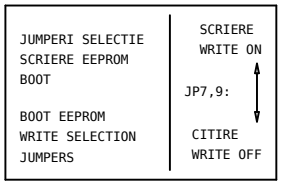




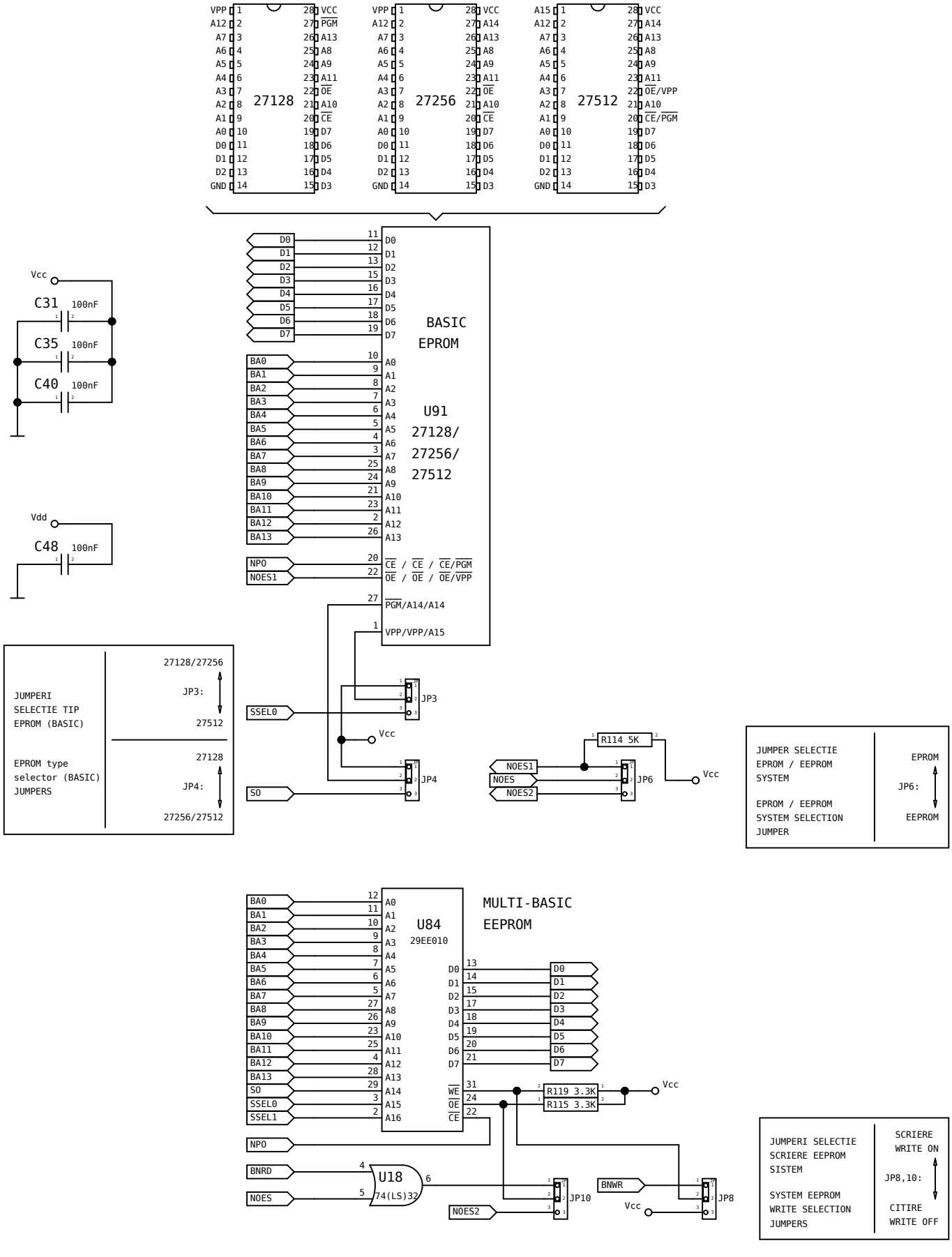




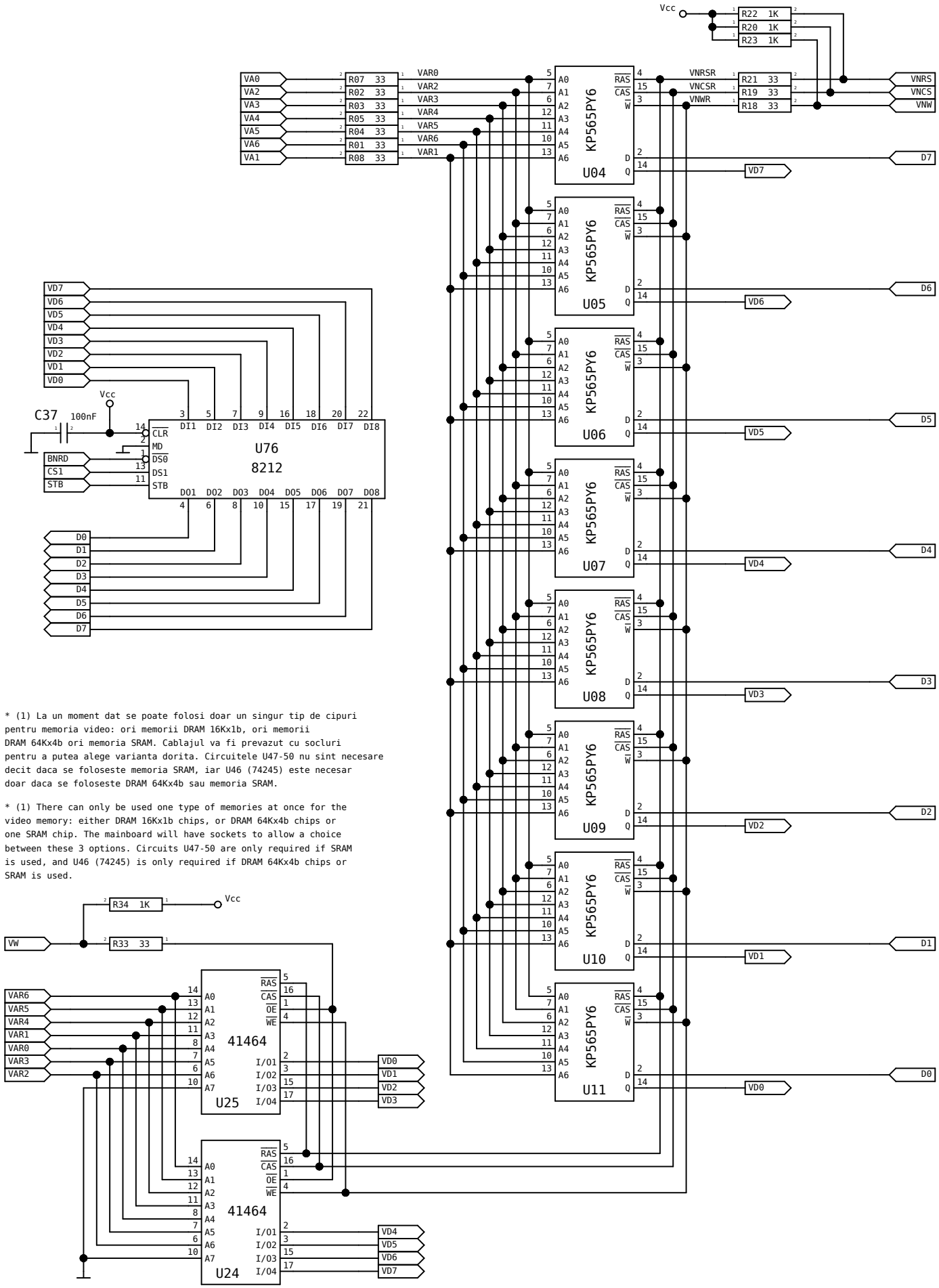




TITLE µC CoBra - Circuitul memoriei nevolatile - pag.1/2 CoBra µC - Read-only memory circuit - pag.1/2	
FILE: CoBra	REVISION: 4.21 (ROM upgrade, 64KB DRAM)
PAGE 10 OF 18	DRAWN BY: ElectroNNix



TITLE μC CoBra - Circuitul memoriei nevolatile - pag.2/2 CoBra μC - Read-only memory circuit - pag.2/2	
FILE: CoBra	REVISION: 4.21 (ROM upgrade, 64KB DRAM)
PAGE 11 OF 18	DRAWN BY: ElectroNNix



* (1) La un moment dat se poate folosi doar un singur tip de cipuri pentru memoria video: ori memorii DRAM 16Kx1b, ori memorii DRAM 64Kx4b ori memoria SRAM. Cablajul va fi prevazut cu socluri pentru a putea alege varianta dorita. Circuitele U47-50 nu sint necesare decit daca se foloseste memoria SRAM, iar U46 (74245) este necesar doar daca se foloseste DRAM 64Kx4b sau memoria SRAM.

* (1) There can only be used one type of memories at once for the video memory: either DRAM 16Kx1b chips, or DRAM 64Kx4b chips or one SRAM chip. The mainboard will have sockets to allow a choice between these 3 options. Circuits U47-50 are only required if SRAM is used, and U46 (74245) is only required if DRAM 64Kx4b chips or SRAM is used.

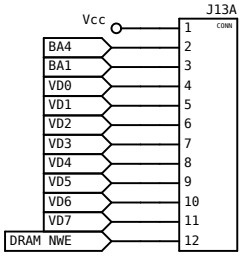
* (2) Memoriile 41464 sint aici folosite la un sfert din capacitate, adica 16KB. Memoriile echivalente de 16K x 4b, adica 4416, au acelasi numar de pini dar multiplexarea adreselor este diferita, asa ca am hotarit sa folosesc 41464 care la ora actuala se gasesc si la un pret mai mic.

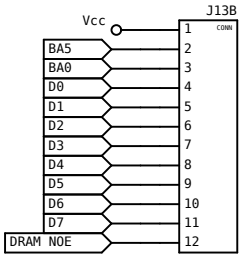
* (2) 41464 are used at 1/4 capacity here, that is 16KB. The equivalent 16K x 4b chips, that is 4416, have the same number of pins but address multiplexing is different, so I decided I will use 41464 which currently are available for a smaller price.

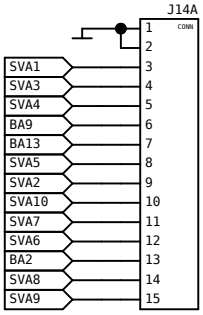
TITLE	µC CoBra - Circuitul memoriei video - pag.1/2 CoBra µC - Video memory circuit - pag.1/2
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 12 OF 18	DRAWN BY: ElectroNNix

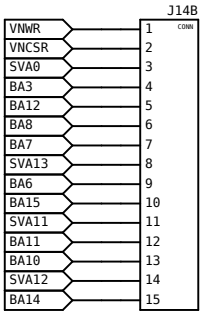
J13A+B, J14A+B
Conectori modul SRAM

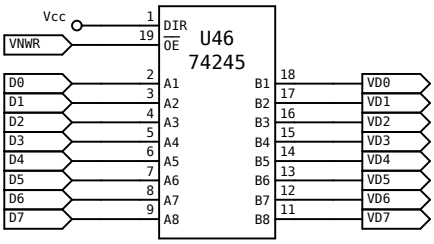
J13A+B, J14A+B
SRAM module connectors











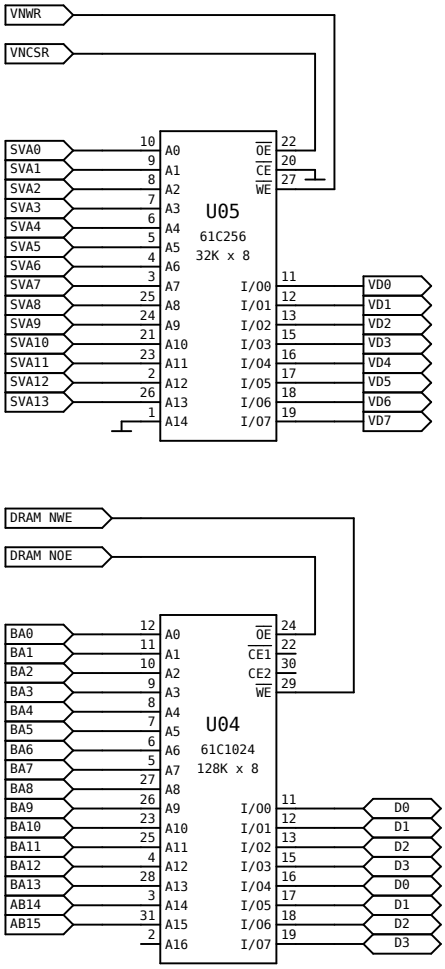
* (2) 74245 are rolul de a conecta magistrala de date la magistrala de date video numai pe durata scrierii de date dinspre procesor in memoria video. In restul timpului liniile de date D0-D7 sint izolate de liniile de date video VD0-VD7. Acest lucru este necesar pentru memoriile DRAM 41464 si pentru memoria RAM statica 61C256, intrucit aceste cipuri nu mai au datele de intrare separate de datele de iesire.

* (2) 74245 has the purpose of connecting the data bus to the video data bus only while the processor writes data to the video memory. In the rest of the time the data lines D0-D7 are disconnected from the video data lines VD0-VD7. This is required for the 41464 DRAM chips and the 61C256 static RAM chip since they do not have data inputs separated from the data outputs.

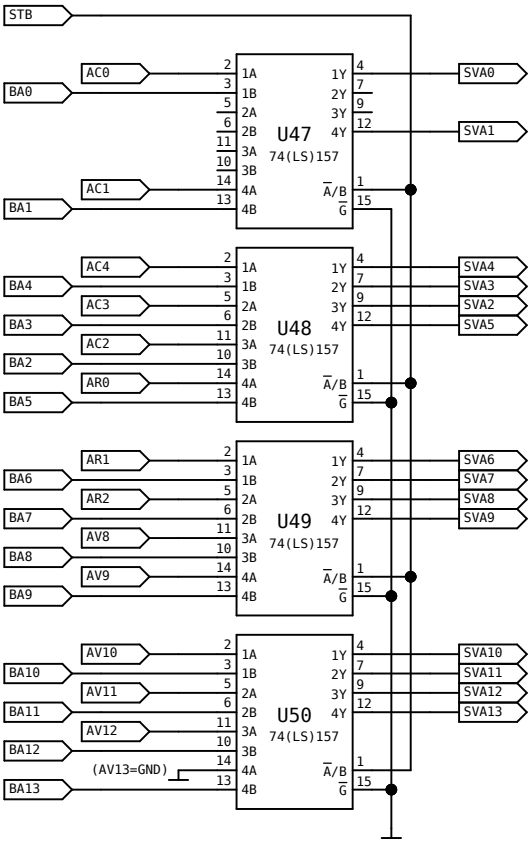
TITLE µC CoBra - Circuitul memoriei video - pag.2/2 CoBra µC - Video memory circuit - pag.2/2	
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 13 OF 18	DRAWN BY: ElectroNNix

* (1) Memoria statica 61C256 este aici folosita la jumatate de capacitate (16KB).
Am folosit acest tip de memorie din doua motive: perspectiva unei eventuale
extensii de memorie si faptul ca memorii mai mici nu am gasit la furnizori.

* (1) The static DRAM chip 61C256 is used here at half its capacity (16KB).
I have chosen this particular chip for two reasons: the perspective of a
possible memory extension and the lack of a 16KB chip from suppliers.



TITLE	µC CoBra - Circuitul modulului memoriei statice CoBra µC - Static memory module circuit		
FILE:	CoBra	REVISION:	4.24 (DRAM upgrade, 64KB DRAM)
PAGE	14 OF 18	DRAWN BY:	ElectroNNix



* (1) U47-50 sint folosite aici pentru multiplexare liniilor de adresa catre memoria video SRAM. Multiplexarea este diferita de cea necesara pentru memoria video DRAM. Spre deosebire de cipurile DRAM, la SRAM nu mai e nevoie de multiplexare intre RAS si CAS, ci doar de multiplexare intre accesul controlerului video si cel al procesorului la memoria video.

Din diagrama din Fig.6 din manualul hardware se observa ca semnalul S0 poate fi folosit pentru a comanda multiplexarea intre adresele pentru RAS si adresele pentru CAS, iar semnalul STB poate fi folosit pentru a comanda multiplexarea intre adresele de la controlerul video si adresele de la procesor. Acest lucru este confirmat de schema originala a multiplexorului de adrese video, avind in vedere ca S0 este legat la bitul inferior de selectie a multiplexoarelor iar STB la cel superior si observind ca adresele de la controlerul video sint legate la intrarile 0 si 1 iar adresele de la procesor sint legate la intrarile 2 si 3.

Rezulta deci ca multiplexarea adreselor pentru SRAM (intre procesor si controler video) poate fi comandata de semnalul STB.

Aceste cipuri nu sint necesare daca nu se foloseste SRAM pentru memoria video.

* (1) U47-50 are used here for address multiplexing to the video SRAM memory. This multiplexing is different than the one required for the DRAM video memory.

Unlike the DRAM chips, SRAM does not require RAS / CAS multiplexing anymore, but only multiplexing between video controller and microprocessor accesses to video memory.

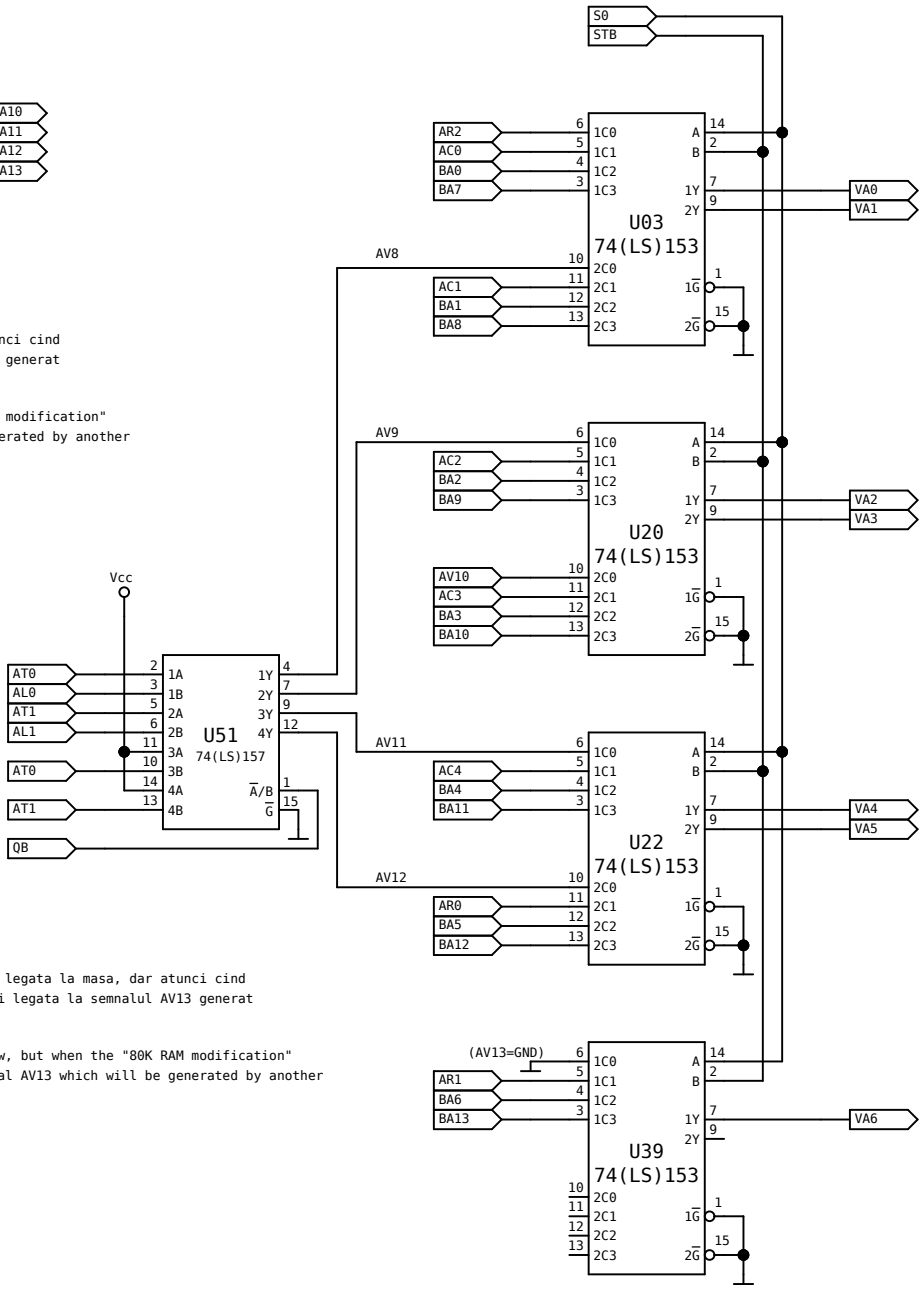
Examining Fig.6 in the hardware manual we can see that signal S0 can be used for driving the multiplexer between addresses for RAS and addresses for CAS, while signal STB can be used for driving the multiplexer between addresses from video controller and addresses from microprocessor. This is actually confirmed by examining the original schematic of the video address multiplexer, considering that S0 drives the lower selection bit of the the multiplexers and STB drives the higher one and noticing that the addresses from the video controller are connected to inputs 0 and 1 and the addresses from the microprocessor are connected to inputs 2 and 3.

In conclusion, address multiplexing for SRAM (between microprocessor and video controller) can be driven by signal STB.

These 4 IC's are not required if SRAM is not being used for the video memory.

* (2) Intrarea U50/14 este deocamdata legata la masa, dar atunci cind se va face "modificarea de 80K" va fi legata la semnalul AV13 generat de un alt circuit.

* (2) Input U50/14 is grounded for now, but when the "80K RAM modification" is done it will be connected to signal AV13 which will be generated by another circuit.



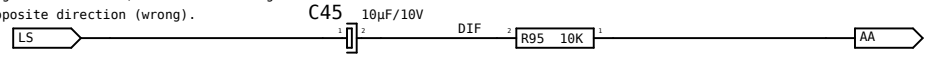
* (2) Intrarea U39/6 este deocamdata legata la masa, dar atunci cind se va face "modificarea de 80K" va fi legata la semnalul AV13 generat de un alt circuit.

* (2) Input U39/6 is grounded for now, but when the "80K RAM modification" is done it will be connected to signal AV13 which will be generated by another circuit.

TITLE	µC CoBra - Circuitul de multiplexare adrese video CoBra µC - Video address multiplexer circuit		
FILE:	CoBra	REVISION:	4.24 (DRAM upgrade, 64KB DRAM)
PAGE	15 OF 18	DRAWN BY:	ElectroNNix

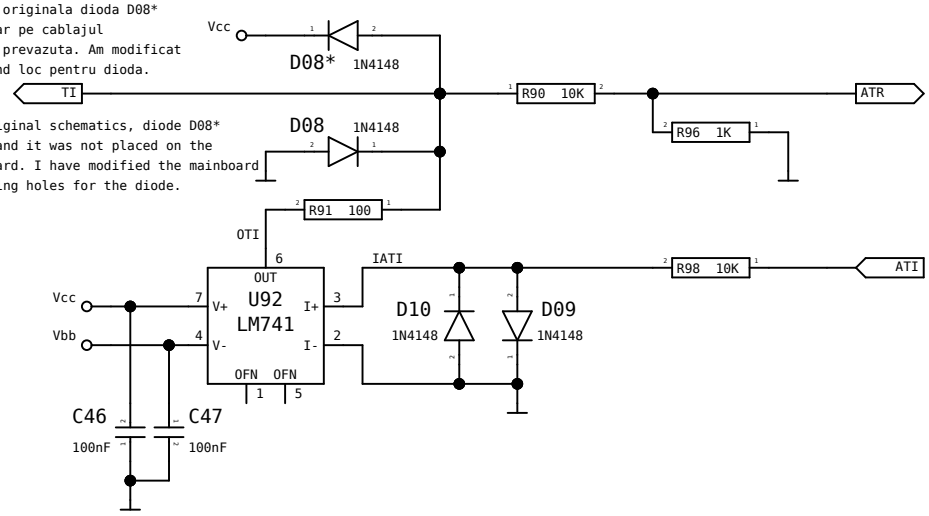
* (1) In schema originala semnalele
LS si AA erau desenate in sens opus (gresit).

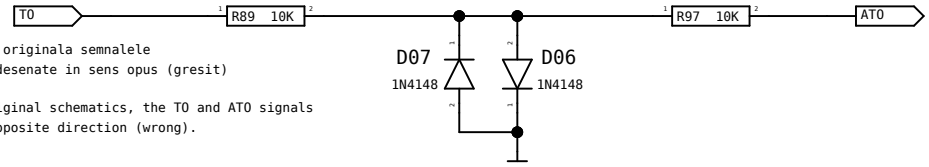
* (1) In the original schematics, the LS and AA signals
were drawn in opposite direction (wrong).



* (2) In schema originala dioda D08*
nu avea nume, iar pe cablajul
original nu era prevazuta. Am modificat
cablajul adaugind loc pentru dioda.

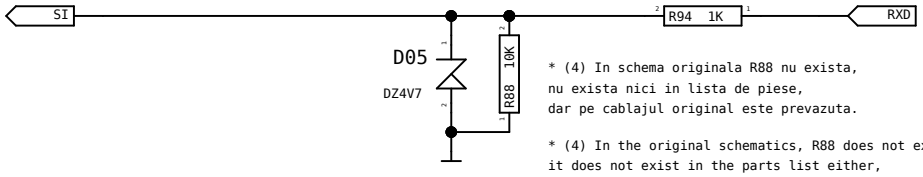
* (2) In the original schematics, diode D08*
was not named, and it was not placed on the
original mainboard. I have modified the mainboard
by adding mounting holes for the diode.





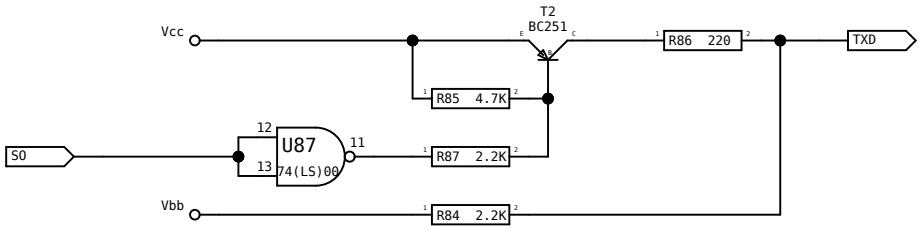
* (3) In schema originala semnalele
TO si ATO erau desenate in sens opus (gresit)

* (3) In the original schematics, the TO and ATO signals
were drawn in opposite direction (wrong).



* (4) In schema originala R88 nu exista,
nu exista nici in lista de piese,
dar pe cablajul original este prevazuta.

* (4) In the original schematics, R88 does not exist,
it does not exist in the parts list either,
but it is placed on the original mainboard.

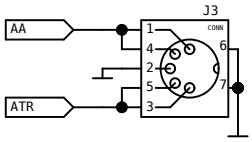


* (5) Pe cablajul original, poarta U87/13,12,11
era intercalata ca inversor intre U85/12 si U86/11,
inversind semnalul I de la U85 la U86 (gresit). Am modificat
deci cablajul conform acestei scheme (originale, corecte).
(Vezi taieturile #1 si #2 de pe fata 1, #20 si #24 de pe fata 2,
si legaturile #18, #20 si #21 de pe fata 2)

* (5) On the original PCB, gate U87/13,12,11 was
placed as inverter between U85/12 and U86/11,
inverting the signal I from U85 to U86 (wrong). I have
therefore changed the mainboard layout according to
the original (correct) schematic (shown here).
(See cuts #1 & #2 on side 1, #20 & #24 on side 2,
and rewirings #18, #20 & #21 on side 2)

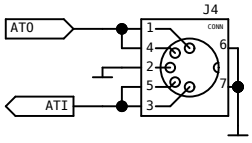
J3 - CONECTOR AUXILIAR

J3 - AUX CONNECTOR



J4 - CONECTOR CASETOFON

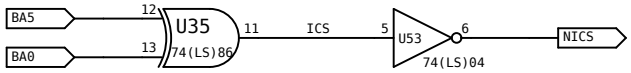
J4 - TAPE CONNECTOR



TITLE µC CoBra - Circuite de adaptare nivel CoBra µC - Voltage-level adapter circuits	
FILE: CoBra	REVISION: 4.21 (ROM upgrade, 64KB DRAM)
PAGE 16 OF 18	DRAWN BY: ElectroNNix

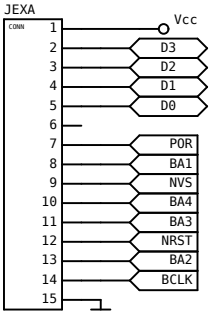
* (1) Pe cablajul original JEXA/8 este legat in mod gresit la BA7.
De asemenea, manualul original avea JEXA/8 listat ca fiind
legat la BA7. Am modificat deci cablajul si
schema de fata legind JEXA/8 la BA1 (corect).
(Vezi taietura #11 fata 1, legatura #22 fata 2)

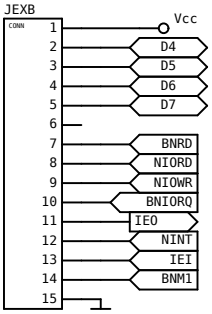
* (1) On the original mainboard, JEXA/8 was connected
(the wrong way) to BA7. Also the original hardware
manual had JEXA/8 listed as being connected to BA7.
I have therefore changed the mainboard layout
and this schematic by connecting JEXA/8 to BA1 (correctly).
(See cut #11 side 1, rewiring #22 side 2)



JEXA+B - CONECTOR INTERFATA
FLOPPY DISK

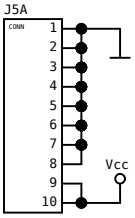
JEXA+B - FLOPPY DISK INTERFACE
CONNECTOR

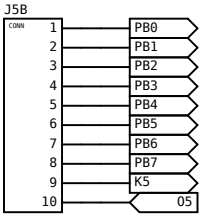




J5A+B - CONECTOR PORT INTRARE
PE 8 BITI ADRESA 0DFH

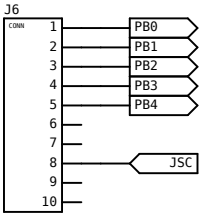
J5A+B - 8-BIT INPUT PORT 0DFH
CONNECTOR

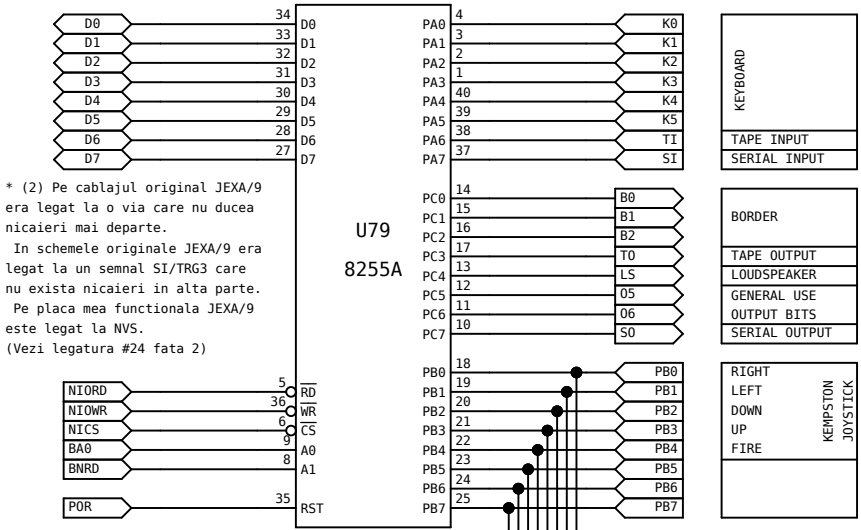




J6 - CONECTOR JOYSTICK
KEMPSTON

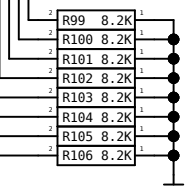
J6 - KEMPSTON JOYSTICK
CONNECTOR



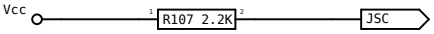


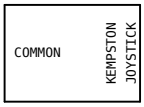
* (2) Pe cablajul original JEXA/9
era legat la o via care nu ducea
nicaieri mai departe.
In schemele originale JEXA/9 era
legat la un semnal SI/TRG3 care
nu exista nicaieri in alta parte.
Pe placa mea functionala JEXA/9
este legat la NVS.
(Vezi legatura #24 fata 2)

* (2) On the original mainboard, JEXA/9 was connected
to a via which was not further leading anywhere.
In the original schematics, JEXA/9 was connected to
a signal "SI/TRG3" which did not exist anywhere else.
On my working mainboard, JEXA/9 is connected to NVS.
(See rewiring #24 side 2)

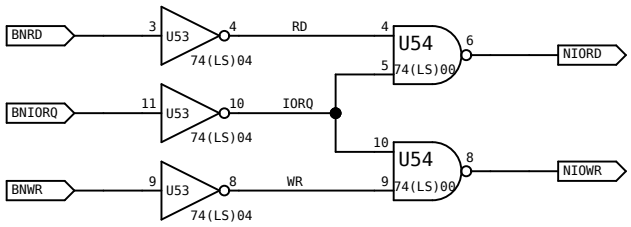


* (3) Pe cablajul original, R107 este legata
in mod gresit la GND in loc de VCC.
(Vezi taietura #13 fata 1, legatura #19 fata 2)



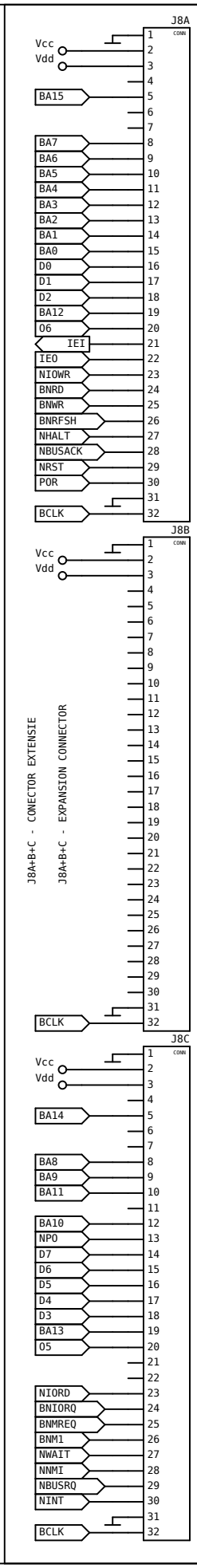


* (3) On the original mainboard, R107 is
wrongfully connected to GND instead of VCC.
(See cut #13 side 1, rewiring #19 side 2)

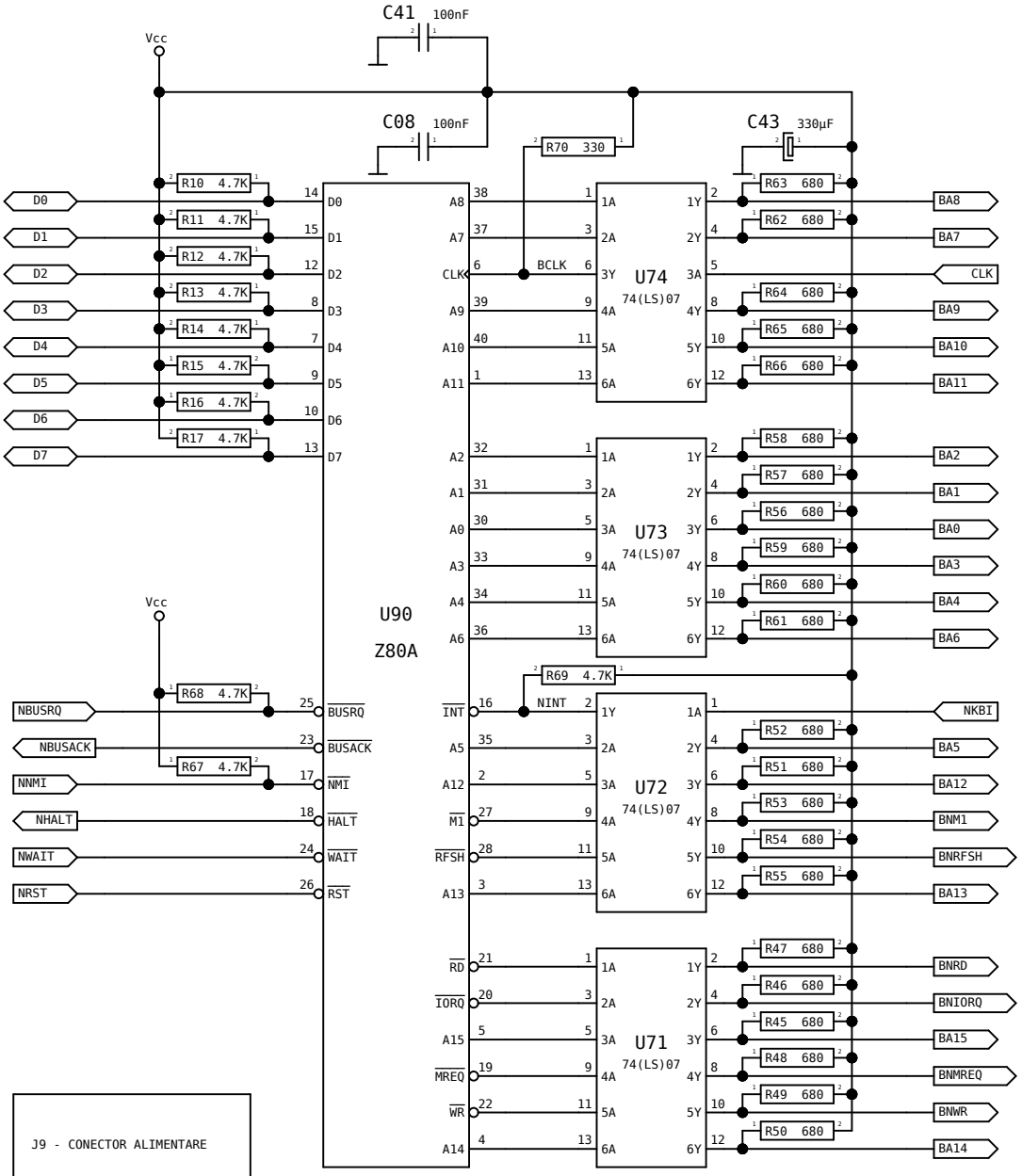


* (4) Cablajul original avea JSC conectat
la J6/pin10 dar manualul original avea JSC
listat la J6/pin8. Am schimbat cablajul placii
de baza pentru a corespunde manualului.
(Vezi taietura #5 fata 1, legatura #1 fata 1)

* (4) The original mainboard had JSC connected
to J6/pin10 but the original manual had JSC
listed at J6/pin8. I changed the mainboard layout
to match the original manual.
(See cut #5 side 1, rewiring #1 side 1)



TITLE μC CoBra - Interfete CoBra μC - Interfaces	
FILE: CoBra	REVISION: 4.21 (ROM upgrade, 64KB DRAM)
PAGE 17 OF 18	DRAWN BY: ElectroNNix

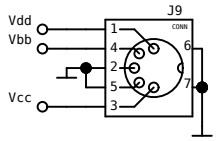


* (1) In schema originala, U74/6 era legat (gresit) la U90/24, dar corect este ca U90/24 sa fie legat la NWAIT, U74/6 (BCLK) sa fie legat la U90/6 (CLK procesor) si U74/5 sa fie legat la CLK

* (1) In the original schematics, U74/6 was connected (wrong) to U90/24, but correct is for U90/24 to be connected to NWAIT, for U74/6 (BCLK) to be connected to U90/6 (CPU clock) and for U74/5 to be connected to CLK

J9 - CONECTOR ALIMENTARE

J9 - POWER CONNECTOR



* (2) In schema originala, R48 lipseste dar este prevazuta in pagina cu dispunerea componentelor pe cablaj

* (2) In the original schematics, R48 is missing but it does exist on the mainboard component placement page

TITLE	µC CoBra - Unitatea centrala CoBra µC - Central Processing Unit		
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	18 OF 18	DRAWN BY:	ElectroNNix